SLAC High Performance System (HPS) and Common Platform

The CPSW is a software layer that provides a common interface to the HPS Common platform FPGA for all high level software.

Communication protocol stack

<table>
<thead>
<tr>
<th>Protocol</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>UDP</td>
<td>Builder</td>
</tr>
<tr>
<td>MPPI</td>
<td>User</td>
</tr>
<tr>
<td>SRP</td>
<td>Developer</td>
</tr>
</tbody>
</table>

APIs

- **Builder**: Assemble hierarchy, define parameters and topology.
- **User**: provide access to a device in the hierarchy.
- **Developer**: All details visible, for defining new objects.

**YAML + CPSW + ASYN: YCPWSYN**

- EPICS module based on asyncPortDriver
- Uses CPSW for accessing the hardware, which is described using YAML.
- General purpose driver, doesn’t have any application specific functions. It gives access to registers and asynchronous messages.
- It has 2 operations mode: auto and manual generation of PVs

Auto-generation of PVs

- In this mode, the module navigates the entire hierarchy defined in YAML and generates PVs for all elements found.
- Based on the type of register and its properties, records of appropriate type are generated and their fields are populated with the register properties defined in YAML (e.g., SCAN, DESC, Bx and MBBx state names, etc.).
- The PV name is generated from the register “path”:

```
fpga/mcis/AccCarrierCore/AccBay0Core/Adc16Dx370[0]/AdcReg_0x0003
```

Manual generation of PVs

- The module gives the possibility to disable the auto-generation and define PV manually for specific registers. This gives the possibility to freely choose PV name and field properties.
- The manual generation of PVs requires 2 steps:
  1. Map a register to an asyn parameter (dictionary file)
  2. Create an appropriate record

```
# Register path
/fpga/mcis/AccCarrierCore/AsxVersion/fpgaVersion
```

```python
async paramete

<table>
<thead>
<tr>
<th>Register information</th>
<th>EPICS PV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register class</td>
<td>Encoding</td>
</tr>
<tr>
<td>IntField</td>
<td>None</td>
</tr>
<tr>
<td>&gt;1</td>
<td>None</td>
</tr>
<tr>
<td>SequenceCommand</td>
<td>N/A</td>
</tr>
</tbody>
</table>

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Abstract:
The Linac Coherent Light Source II (LCLS-II) is a major upgrade of the LCLS facility at SLAC, scheduled to start operations in 2020. The High Performance Systems (HPS) defines a set of LCLS-II controls sub-systems which are directly impacted by its 1MHz operation. It is formed around a few key concepts: ATCA based packaging, digital and analog application boards, and 10G Ethernet based interconnections for controls. The Common Platform provides the common parts of the HPS in term of hardware, firmware, and software. The Common Platform Software (CPSW) provides a common interface to the common platform’s FPGA for all high-level software. YAML is used to define the hardware topology as and all necessary parameters. YCPWSYN is an AsynDriver based EPICS module for FPGA register access and asynchronous messaging. It uses CPSW for accessing the hardware which is described by YAML. YCPWSYN has two operation modes: an automatic mode where PEs are automatically created for all registers and the record’s fields are populated with information found in YAML; and a manual mode where the engineer can choose which register to expose via PEs and freely choose the record’s filled information.

The Linac Coherent Light Source II (LCLS-II)

LCLS is the world’s first hard X-ray free-electron laser. Its strobe-like pulses are just a few millimeters of a billionth of a second long, and a billion times brighter than previous X-ray sources. Scientists use LCLS to take crisp pictures of atomic motions, watch chemical reactions unfold, probe the properties of materials and explore fundamental processes in living things.

LCLS-II will provide a major jump in capability – moving from 120 pulses per second to 1 million pulses per second. This will enable researchers to perform experiments in a wide range of fields that are now impossible. The unique capabilities of LCLS-II will yield a host of discoveries to advance industry, new energy solutions and our quality of life.

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**SLAC High Performance System (HPS) and Common Platform**

Due to the 1MHz operation rate of the LCLS-II, SLAC is implementing the High Performance System which is based on ATCA. Each application controls will be implemented in one ATCA blade. The carrier card provides the FPGA as well as all the digital and power sections which are common to all applications. The analog application-specific sections are in the AMC daughters card.

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**SCALABLE FPGA VERSIONING**

- **Builder**: Assemble hierarchy, define parameters and topology.
- **User**: provide access to a device in the hierarchy.
- **Developer**: All details visible, for defining new objects.

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**Accessing the registers using the user API**

- Load hierarchy description
  - Path root + DRMA: LoadFamFile(file.yaml);
- Navigate the hierarchy (lookup)
  - Path p = root + findByPath("fpga/mcis/AccCarrierCore/AsxVersion/fpgaVersion");
- Access properties
  - IntField.get(1).get1().get2().get3().variable();
- Access properties
  - IntField.get(1).get1().get2().get3().variable();

---

**Multi-accessable User Interface**

- Scalable fpgaVersion = this:fpgaVersion:remote();
- fpgaVersion.get1().get1().get2().get3().variable();