A time stamping TDC for SPEC and ZEN platforms based on White Rabbit

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Sub-nsec precision time synchronization is requested for data-acquisition components distributed over up to tens of km² in modern astroparticle experiments, like upcoming Gamma-Ray and Cosmic-Ray detector arrays, to ensure optimal triggering, pattern recognition and background rejection. The White Rabbit (WR) standard for precision time and frequency transfer is well suited for this purpose. We present two multi-channel general-purpose TDC units, which are firmware-implemented on two widely used WR-node: the SPEC (Spartan 6) and ZEN (Zynq) boards. Their main features: TUG with 1 ns resolution (default), running deadtime-free and capable of local buffering and centralized level-2 trigger architectures. The TDC stamp pulses are in absolute TAI. With off-the-shelf mezzanine boards (SCHIO-FMC-modules), up to 5 TDC channels are available per WR-node. Higher density, customized simple I/O boards allow to turn this into 8 to 32-channel units, with an excellent price to performance ratio. The TDC units have shown excellent long-term performance in a harsh environment experiment at TAIGA-HISCORE/Siberia, for the front-end DAQ and the central GPSDO clock facility.

White Rabbit

• Sub-nanosecond precision timing system
• Delivers absolute TAI time at every WR node
• Fully deterministic Ethernet-based network for data transfer and synchronization
• Open Source Hard-, Firmware, and Software

White Rabbit Nodes SPEC and ZEN
We focus on firmware implementation of commercially available WR nodes to typical physics applications for time stamping and DAQ control

Field Application: TAIGA HISCORE
• Cosmic- and gamma rays emit Cherenkov light detectable on ground
• Multiple detectors distributed over a large area 1km²-10km²
• 28 station prototype (0.25km²) operating in Tunka, Siberia
• Each station detects Cherenkov light with 4 PMTs
• Astronomical pointing of <0.1° requires pulse timestamps with <1ns accuracy

Conclusions
• Basic implementation of a 1 ns TDC: Deadline free, absolute TAI, no trigger necessary
• Integrated in 3 different variations: single channel TDC w/ DAQ control, 4 channel TDC, and 1 channel 0.25s sampling TDC on the SPEC WR node
• Easily extendable to more channels with a simple custom board
• 1 ns TDC implemented and running in HISCORE
• 4 channel TDC as White Rabbit timing monitoring system

White Rabbit Nodes: TDC Firmware Design
Basic TDC design
• Developed a 1ns sampling TDC
• SOC DIO has adjustable input thresholds for analog input options
• On input signal save time stamp in a CPU accessible FIFO
• Delivers deadline free TAI time stamps
• No external trigger needed
• Easy to implement
• Input/Output channels can be easily be adapted for any trigger and DAQ control requirements

TDC Implementation: SPEC WR node
• TDC attached to the Wishbone bus
• Software assembles UDP Packets
• Realized with SPEC board
• Easy White Rabbit System Monitoring

TDC Implementation: ZEN WR node
• Linux running ARM core reads out FIFO
• Software assembles UDP Packets
• High time stamp read out rate of >100 kHz
• Default TDC sampling rate 1ns (Speed Grade -3) and 2ns (2)

Multichannel TDC

4 Channel TDC
• 4 TDC integrated in the SPEC FPGA
• Timestamp independently for each channel
• Realized with SPEC board
• Easily extendable to more TDC channels
• With a simple custom DIO board

4 TDC Example Application
• Easy White Rabbit System Monitoring
• Sample PPS signals of several WR devices
• Multiple clock verification

High Resolution TDC
• Split incoming signal and feed it into 4 individually delayed TDCs
• External fanout can be implemented in a simple DIO card
• Logic creates high resolution timestamp
• Implemented with SPEC board
• Expected better performance with ZEN board due to temperature compensated IDELAYs

References

Wir schaffen Wissen – heute für morgen

Multichannel TDC

1 Ch High Res TDC

Using an external fanout and the IDELAYs of the FPGA increases the Time Stamp resolution to 20 ps.