The CERN LHC central timing
A vertical slice

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Talk layout

- LHC Injector Chain Timing
- Timing Distribution Overview
- Central Timing Overview
- Reflective Memory
- UTC Time and GPS
- The Multitask Timing Generator
- The Controls Timing Receiver Module
- Safe Machine Parameters Hardware Checking
- LHC Software Architecture and Event Tables
The LHC Proton Injector Chain
Strongly time coupled
CERN accelerator network sequenced by central timing generator
CERN accelerator network sequenced by central timing generator
CERN accelerator network sequenced by central timing generator
CERN accelerator network sequenced by central timing generator
CBCM Sequence Manager
The LHC Beam

The LHC timing is only coupled by extraction

LHC Injection plateaux

Injection

Extraction

Extraction Forewarning

SPS injection plateaux

SPS Cycle for the LHC

CPS Batch 1
PSB1
PSB1

CPS Batch 2
PSB2
PSB2

CPS Batch 3
PSB3
PSB3

CPS Batch 4
PSB4
PSB4

LSA Beam request:
RF bucket
Ring
CPS batches

start-ramp event
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Timing Distribution Overview

- RS485 drop nets distribute timing around the CERN accelerator complex
- Long distance transmission over optical fibers
- One timing network for each accelerator
- Hundreds/Thousands of timing receiver modules distributed around the complex
- One timing generator drives one timing network
Timing Frames

- Timing frames are Manchester encoded at 500kbit using a 1MHz clock.
- Each frame carries 32 data bits, parity, start and stop bits.
- One frame transmitted each 125μs, 8 per millisecond.
- The frame data is broken into bit fields
  - 4 Bits Accelerator [A]
  - 4 Bits frame Type [T]
  - 8 Bits Code [CODE]
  - 16 Bits Payload [PAYLOAD]
- Some frames are recognized by the hardware and cause special treatment
  - Two UTC frames carry the time of day in their payload
  - Millisecond frames are always sent in phase with the PPS
  - Telegram frames are stored in double buffers
  - Event frames cause counters to be loaded and triggered and may produce bus interrupts
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Reflective Memory

LHC Timing generator A

Identical except
ID event

LHC Timing generator B

2Gbit/S
Token ring

VMIACC-5595
Single Mode
Hub

P0RTS token ring

64Mbyte
VMIPMC-5565
Reflective memory

LHC Gateway
Implements FESA API

Reflective memory:
A and B must always be
in the same state.
If no restrictions for
switch over
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Multitask Timing Generator MTT

- Hardware multitasking for 16 tasks
  - 32 local registers per task
  - 218 Global registers
  - 6 Memory mapped IO registers
    - Timing frame out register
    - VME P2 in register ...
- Host processor access to all registers

- Implements general purpose CPU
  - Op-codes are triadic: AND SrcREG,SrcREG,DstREG – AND 0x7,VMEP2,TMP
    - Arithmetic and logical
    - Move indexed, literal, register
    - Wait value, relative
    - Conditional branch
    - Interrupt host
- Tasks defined from host via Task Control Block
  - PC
  - PC Offset
  - Processor Status Word
- Command and status registers allow host access to running tasks
MTT hardware module

See: The LHC central timing hardware implementation
P. Alvarez, J. Lewis, J. Serrano CERN, Geneva, Switzerland

This conference
MTT External Events Task

- **strt:**
  - `% Start program and interrupt survey task`
  - `movv TskStsRUNNING LRegTASK_STATUS`  `% Say we are running`
  - `movv ConsNOT_SET LRegParRUN_COUNT`  `% Run forever`
  - `int 2`  `% Notify survey we are running`

- **cont:**
  - `% Wait for the VME P2 bits and send out events accordingly`
  - `movv ConsVMBP2_BITS VMEP2`  `% Wait for VME P2 bits`
  - `movv VMEP2 RegVmeP2`  `% Copy reg and clear bits`

- **tdmp1:**
  - `% Test for dump ring 1`
  - `andv ConsHX_DMPD1_BIT RegVmeP2 LRegTEMP`  `% Test dump 1 bit`
  - `beq tdmp2`  `% Go check for dump 2 bit`
  - `movv ConsHX_DMPD1 EVOUT`  `% Send dump 1`
  - `movv ConsHX_ENBPM1 EVOUT`  `% Re-enable after a dump`

- **tdmp2:**
  - `% Test for dump ring 2`
  - `andv ConsHX_DMPD2_BIT RegVmeP2 LRegTEMP`  `% Test dump 2 bit`
  - `beq tinj`  `% Go injection warning bit`
  - `movv ConsHX_DMPD2 EVOUT`  `% Send dump 2`
  - `movv ConsHX_ENBPM2 EVOUT`  `% Re-enable after a dump`

- **tinj:**
  - `% Test for LHC injection`
  - `andv ConsHX_FM_BIT RegVmeP2 LRegTEMP`  `% Test inject bit`
  - `beq tpml`  `% Go check for PM ring 1`
  - `movv ConsHX_FM EVOUT`  `% Send injection forewarning`

- **tpml:**
  - `% Test for post mortem bit 1`
  - `andv ConsHX_PM1_BIT RegVmeP2 LRegTEMP`  `% Test PM ring 1 bit`
  - `beq tpml2`  `% Go check for PM ring 2`
  - `movv ConsHX_PM1 EVOUT`  `% Send PM-1 trigger`

- **tpm2:**
  - `% Test for post mortem bit 2`
  - `andv ConsHX_PM2_BIT RegVmeP2 LRegTEMP`  `% Test PM ring 2 bit`
  - `beq cont`  `% Go check for PM ring 2`
  - `movv ConsHX_PM1 EVOUT`  `% Send PM-1 trigger (not PM-2)`

- **jmp cont:**  `% Go wait for next P2 interrupt`
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Controls Timing Receiver CTR

Hybrid PLL

Delay

Content Addressed Memory - Triggering

40MHz

Frame Decoder

22Bit 50MHz Counters

Bus Interrupt

Counter Configurations Loader

Load

Output

Start
- Previous
- External
- Event

Clock
- Previous
- 40MHz harmonic
- External

Modes
- Once
- Multi-pulse
- Burst

Trigger
- Event frame
- Wildcard
- Telegram

Action
- Output
- Bus interrupt

Output
- TTL/TTL bar
- Pulse width

CTRV – CTRI – CTRP formats
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Safe Machine Parameters Distribution

- SMP @ 10Hz 16Bit $10^{10}$ (Flags, E & Int.)
- Events, UTC, & Telegrams (including SMP)
- Flags TTL Hw Output
- LHC Timing Generator
- Safe Machine Parameters Controller for LHC
- Energy A
- Energy B
- BCT "A"
- BCT "B"
- L_beam1 & 2
- BEM
- BEM
- CTRx
- CTRV
- CTRV
- CTRV
- Kickers
- BLM
- EXP
- EXP
- If length > 5m
- Reads thresholds
- Reads status
- Management Critical Settings
- LSA
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LSA and FESA

- The FESA API is implemented on the LHC timing gateway
- Accesses timing generators across reflective memory
- Implements
  - Load or Unload event table
  - Get running tables list
  - Set event table run count and synchronization event
  - Stop or Abort event table
  - Set telegram parameters
  - Send event
  - Read status of tasks and MTT module
Conclusion

- Event tables model LHC machine processes.
- Reuse of existing timing boards was facilitated by using FPGAs and writing new VHDL.
- The LHC timing is monitored by hardware.
- Reflective memory has increased reliability.