

DIGITAL SIGNAL PROCESSING TECHNIQUES TO MONITOR BUNCH-BY-BUNCH BEAM POSITIONS IN THE LHC FOR MACHINE PROTECTION PURPOSES

J. Pospisil*, O. Bjorkqvist, A. Boccardi, M. Wendt, CERN, Geneva, Switzerland

Abstract

This paper presents the development of an upgrade to the beam position interlock system for the Large Hadron Collider (LHC) at the European Organization for Nuclear Research (CERN). The beam orbit at the beam dump kicker is continuously monitored by 16 beam position monitors that are part of the machine protection system. In case of unacceptable orbit movement the system has to trigger the beam abort immediately to prevent damage to the machine. An upgrade of the present system is underway with the aim of handling a larger dynamic range of bunch intensities, and coping with different bunch time structures (both the standard bunch spacing of 25 ns and special doublet bunches spaced by 5 ns).

The proposed architecture combines the analogue signals from opposite pickup electrodes on a single read-out channel, and stretches it with a delay-line based comb-filter. The resulting signal, covering a dynamic range of 60 dB, is digitized at 3.2 GSa/s and processed inside a Field-programmable Gate Array (FPGA) to extract a position value. Different signal processing techniques are compared on simulated ideal beam signals, and preliminary results of a prototype installation is presented.

INTRODUCTION

The interlock Beam Position Monitor (BPM) system is used to protect the aperture of the two LHC beam dump channels (one for each beam) by ensuring that the position of the circulating beam never exceeds what is considered to be a safe value whenever a beam dump is requested. It continually monitors the beam position of all bunches and will itself trigger a beam dump if the beam position lies outside a ± 3.5 mm window for a predefined number of bunches over a predefined number of turns (linked to expected damage thresholds with respect to beam intensity and energy). It comprises 16 stripline BPMs, and at present is read-out using the standard *Wide-Band Time Normalizer* (WBTN) LHC position system electronics combined with dedicated FPGA firmware [1, 2]. This system performs bunch-by-bunch position measurements with a nominal resolution ranging from 150 μm to 50 μm , while covering a respective range of bunch intensities from 2×10^9 to 1.5×10^{11} charges per bunch (cpb). This is achieved using two sensitivity settings, one from 2×10^9 to 5×10^{10} cpb and the other from 2×10^{10} to 1.5×10^{11} cpb. The current system has several downsides:

- The need to switch sensitivity means that the system cannot effectively operate with bunches of very different intensity in the machine at the same time.
- The system suffers from performance degradation due to temperature drifts.
- The limited flexibility in terms of beam filling patterns, requiring a minimum bunch-to-bunch spacing of 25 ns.

This latter point is a major limitation for beam scrubbing runs, when the LHC is filled with 5 ns so-called “doublet bunches”, i.e. a pair of bunches spaced by 5 ns, themselves spaced by a 25 ns from the next pair [3]. This operational mode and the other limitations mentioned call for a new read-out system for the LHC interlock BPMs.

SINGLE CHANNEL DIGITIZATION

In the proposed architecture shown in Fig. 1, the signals from both electrodes are time multiplexed onto a single read-out channel using a 12.5 ns delay transmission-line, Delay Multiplex Single Path Technology (DMSPT), where some minimum signal conditioning is applied before the conversion to the digital domain. This analog RF signal conditioning is limited to a delay-line based band-pass comb filter, an anti-aliasing low-pass filter and gain/attenuator stages. Most of the processing then takes place in a subsequent FPGA.

The two main advantages of this architecture are the direct digitization, which allows doublet bunches to be processed, and the single channel read-out scheme, which reduces beam position offset effects caused by asymmetries in the signal processing electronics [4–6].

Analog Signal Processing

The single bunch response from a stripline electrode is a bipolar pulse, which in the case of the LHC is, to first approximation, a single 500 MHz sinusoidal oscillation of ~ 2 ns duration. A band-pass comb filter, operating at the same central frequency combines four time-shifted replicas of the input signal from opposite electrodes to generate two ~ 8 ns sine-wave like bursts of four oscillation periods at 500 MHz. This can be seen in Fig. 2a with results of a beam measurement performed in the Super Proton Synchrotron (SPS) on a single bunch. In this case the ADC was running at 3.2 GSa/s giving up to 30 usable samples per electrode to reconstruct the signal amplitudes.

In the case of doublet bunches only some parts of each 8 ns bursts are unaffected by the doublet structure leaving only ~ 10 samples for signal reconstruction, see Fig. 2b.

* j.pospisil@cern.ch

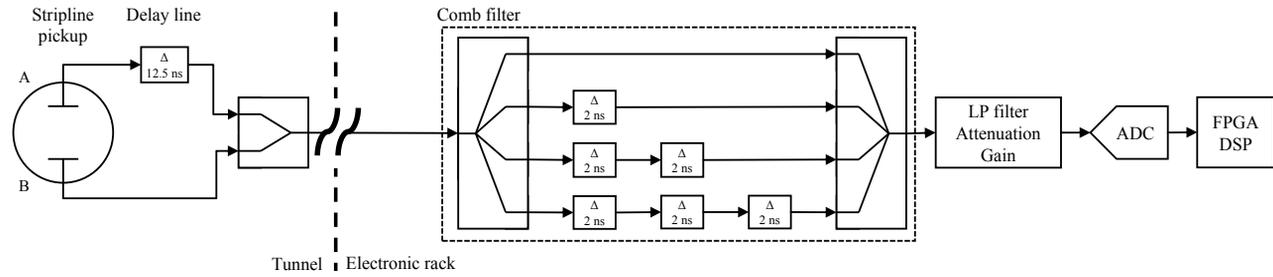
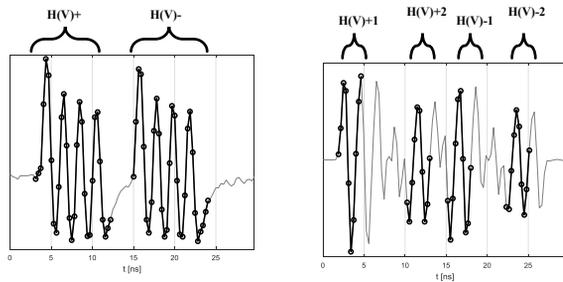


Figure 1: Overall scheme.

Digital Signal Processing

A circuit simulation of the analog front-end defined a 1.2 GHz high cut-off for the analogue processing bandwidth of the ADC to limit effects from signal ringing. This results in a minimum sampling rate of 2.5 GSa/s, assuming no undersampling. Decimation, normalization and calculation of the beam position is performed in real-time, bunch-by-bunch, using an FPGA.

The digital part of the system will be clocked asynchronously to the machine clock, to be able to operate fully independently from any external clock signals (a requirement of the machine protection system).



(a) Single bunch (measured). (b) Doublet bunch (simulated).

Figure 2: Band-pass filtered signal, as seen by the ADC.

PERFORMANCE ESTIMATION

A MATLAB framework was developed to simulate the BPM signal processing, and to evaluate the overall performance of the system. In this framework a signal generator module simulates the ADC output signal, based on an electromagnetic analysis of the stripline BPM combined with a circuit analysis of the analog front-end. Several parameters, like beam intensity and position, sampling time-shift, and ADC characteristics (noise, sampling frequency and number of bits per sample) can be varied and optimized. The second part of the simulation framework evaluates different signal processing algorithms to extract the bunch-by-bunch beam position, while in the final part the simulated results are compared for a variety of initial beam parameters.

Amplitude Extraction Algorithms

The beam position of each bunch is computed by comparing the intensity normalized amplitudes of opposite pickup

electrodes:

$$\text{BeamPosition} = k \frac{A_+ - A_-}{A_+ + A_-}$$

where A_+ , A_- are the amplitudes of the sampled waveforms of the processed electrode signals and k is a non-linear calibration function defined by the pickup geometry. In our case k can be considered a constant equal to 0.79 dB/mm, equivalent to a $\sim 1\%$ signal modulation for a beam displacement of 100 μm . Different algorithms have been tested and compared using the simulation framework to obtain A_+ and A_- from the raw ADC samples, including integration, analysis in the frequency domain, time and frequency convolution, and fitting algorithm. A simple, Root Mean Square (RMS) analysis turned out to be the best compromise between complexity and performance, where the signal amplitude is computed as:

$$A = M \cdot \sqrt{\frac{1}{n} \sum_{i=1}^n s_i^2}$$

where M is a calibration factor, n is number of samples and s_i is the i^{th} waveform sample.

Simulation Results

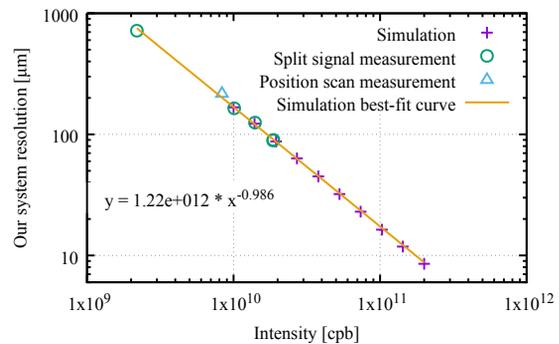


Figure 3: Position resolution from simulations and measurement campaigns obtained using the RMS algorithm.

The parameters of the initial MATLAB simulations are based on the characteristics of the ADC used for prototyping this BPM system: the ~ 9 Effective Number of Bits (ENOB) 4 GSa/s Texas Instruments ADC12J4000 [7]. Figure 3 shows preliminary estimations of achievable resolution vs. bunch

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intensity from both simulations and beam measurements performed in the SPS for the single bunch case. Simulation studies showed no measurable dependency of the position resolution on the sampling phase (time) with respect to the signal, and only a minor degradation for beams with large displacements (± 7.5 mm). For a signal varying in amplitude by a factor of 20, covering almost the full-scale input range of the ADC, the single bunch position resolution ranges between $9 \mu\text{m}$ and $167 \mu\text{m}$. Further simulation studies showed that the noise floor of the ADC remains the dominant limitation, with each additional ENOB improving the resolution by a factor 2. The same result could also be achieved by increasing the sampling frequency by a factor of 4.

PROTOTYPE PERFORMANCE

A prototype setup of the BPM signal processing chain similar to the layout shown in Fig. 1 was assembled for testing on a button-type BPM pickup in the SPS. The delay-line components used for the band-pass comb filter were made from connectorized RF power combiners/splitters and semi-rigid coaxial cables. For the ADC a commercial FMC mezzanine board *Vadatech FMC225* [8] was hooked to an in-house developed VME carrier board [9] holding an *Altera Arria V GX* FPGA for the digital signal processing. The 4 GSa/s sampling rate of the ADC board had to be reduced to 3.2 GSa/s, a limit set by the data links to the FPGA.

Beam Measurements

Two measurement campaigns were performed, both looking only at the vertical plane and using single bunches. Even though the BPM pickup and bunch parameters differ slightly from those of the LHC interlock BPM, the signals generated are nevertheless very similar.

In the first measurement campaign, only one electrode was used with the signal split to simulate two independent electrode signals. In this way the beam displacement could be simulated independently from the actual beam orbit in the machine by inserting various RF attenuators. The dispersion of the long coaxial cables between beam pickup and electronics, and some residual ringing of the comb filter, resulted in some coupling between successive 8 ns burst waveforms and between consecutive bunches (see Fig. 4). This causes a position shift for the subsequent bunches which is in the order of the resolution of the system. The position resolution obtained from this measurement, applying the RMS algorithm, is inserted into Fig. 3 and agrees very well with the simulations.

In the second set of measurements, both electrodes were connected and a real beam position scan was performed. The beam orbit was altered in several steps over a range of ~ 6 mm, while monitoring the beam position with both the prototype BPM system and with operational SPS BPM system [10, 11]. Figure 5 shows a comparison of the acquired position scans. A very good agreement is observed with little change in resolution over this range of positions.

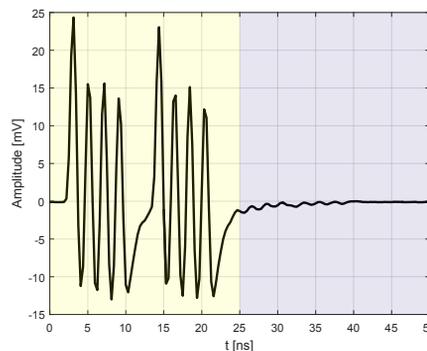


Figure 4: Inter-electrode and inter-bunch coupling shown for a single bunch (25 ns bunch boundaries highlighted).

The resolution of the prototype should not be directly compared to the one of the operational SPS system as the marked uncertainty for the prototype system refers to a bunch-by-bunch, single pass measurement, while for the operational system it is the residual noise after an average of 1 ms for all bunches in the machine. Moreover, the prototype was missing a gain stage, resulting in an equivalent intensity below the target measurement range.

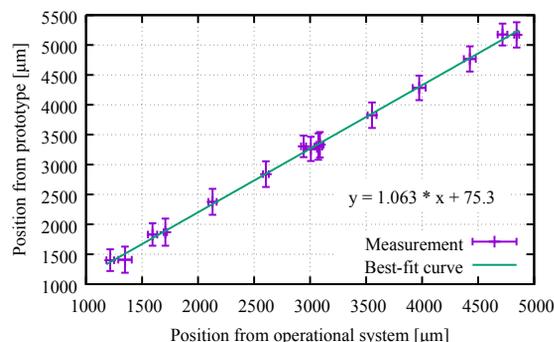


Figure 5: Position scan in the SPS comparing the prototype system to the operational BPM system.

CONCLUSION

A new bunch-by-bunch beam position monitoring system for the beam dump interlock of the LHC, based on a single-channel read-out scheme followed by direct digitization, has been presented. The estimation of BPM performance based on simulations showed the single-bunch, single-pass resolution to be in the range $9 \mu\text{m}$ to $167 \mu\text{m}$ for a position displacement up to ± 7.5 mm, and an intensity from 1×10^{10} to 2×10^{11} cpb in a nominal filling scheme with 25 ns spaced bunches. This is in agreement with the initial results from beam measurements using a prototype installation in the SPS.

Additional studies need to be performed to characterize the proposed system for doublet bunch operation. The resolution is expected to be lower compared to that for nominal bunch spacing, but is still expected to be fully compatible with the interlock system requirements.

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