CERN’s FMC kit

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Outline

1. Why a new kit
2. Introduction to Open Hardware
3. Open Hardware products
4. Gateware architecture
5. New tools
6. Future work & conclusions
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## CERN Beams Controls group

### Responsible for
- Specification, design, procurement and operation of electronic modules
- Linux device drivers, C/C++ libraries, test programs

### Hardware kit
- Analog and digital I/O
- Level converters, repeaters
- Serial links, timing modules

### Currently, October 2013
- About 120 module types
- Most are custom designed: only 1 in 4 is commercial
Why a new kit?

Motivations to design a new kit

- Obsolete components/modules → can’t build/buy
- Limited stock → no new installations
- Incomplete/nonexistent documentation

New approach

- Open and modular designs
- Compliant with existing standards

Carrier-mezzanine concept

- Only one complex design per platform (carrier)
- Reduce number of supported modules
Use of standards

Based on standards

- Platform bus: VME, PCI, PCIe, PXIe
- FMC (FPGA Mezzanine Card, ANSI/VITA 57.1)
- Wishbone FPGA internal bus
- Linux device drivers

Contribute to standards

- FMC bus Linux driver structure: in Linux v3.11
- ZIO Linux framework for DAQ and CTL hardware: RFC made to Linux Kernel list
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Why we use Open Hardware

- Fully specify the design
  - Avoid black boxes.

- Better designs
  - Peer review by experts, including companies.

- Knowledge sharing by design re-use
  - One of CERN’s key mission.
  - Stimulates collaborations, inside and outside CERN.

- Healthier relationship with companies
  - No vendor-locked situations.
  - Small companies can play important role.
Open Hardware Repository – ohwr.org

- Web-based collaborative tool for electronics designers
- Wiki, File repository, Issues management, Mailing list, News
- Readable by everyone, without registration

CERN Open Hardware License – ohwr.org/cernohl

- Developed by Knowledge Transfer Group at CERN.
- Better suited than non-HW licenses (GPL, Creative Commons. . . )
- Defines conditions for using and modifying licensed material.
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## Open Hardware products

### More than just a board
- Hardware board
- FPGA gateware
- Linux driver
- Production test system

### Carriers
- Three fully supported (VME, PCIe, PXIe)
- Six other carriers (VXS, AMC, stand-alone)

### Mezzanines
- Four fully supported (ADC-100M, TDC, DIO-5ch, FD)
- About a dozen other mezzanines (ADC, DAC, DDS, DIO)
SVEC - Simple VME FMC Carrier
Commercialised in Germany
SPEC - Simple PCI Express FMC carrier
Commercialised in Spain, The Netherlands & Poland
SPEXI - Simple PXI Express FMC carrier
A modified SPEC board
FMC mezzanine: 5-channel 1ns TDC
A joint development by TE/ABT, TE/CRG & BE/CO
FMC mezzanine: 100 MSPS 14-bit 4-channel ADC
### Commercially available CERN OH designs

September 2013

<table>
<thead>
<tr>
<th>Project</th>
<th>Producers</th>
<th>Users</th>
<th>Produced</th>
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<tbody>
<tr>
<td>SPEC carrier - PCIe</td>
<td>3</td>
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<td>SVEC carrier - VME</td>
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<td>4</td>
<td>105</td>
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<td>SPEXI carrier - PXIe</td>
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<td>2</td>
<td>(proto) 3</td>
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<td>TDC 1ns 5cha</td>
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<td>FMC DEL 1ns 4cha</td>
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<td>FMC DIO 5ch</td>
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<tr>
<td>WR switch 18 ports</td>
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</table>

**Table:** eight CERN OH designs found producers and users
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Gateware architecture

Wishbone for modularity
- Open standard
- Simple, uses few FPGA resources
- Collection of cores already available (OpenCores)

New cores developed
- At CERN: VME64x, PCIe, DDR3, ...
- By collaborators: Wishbone crossbar (GSI), ...
Example: FMC-ADC gateware architecture

- ADC core
- SPI master
- I2C master
- I2C master
- Memory controller
- Time-tag core
- Interrupt controller
- DMA ctrl
- PCIe ctrl & stat
- 1-wire master
- FMC connector
- FMC-ADC mezzanine
- PCIe carrier
- DDR3 memory 256MB
- DMA ctrl
- PCIe core
- Wishbone crossbar
- Wishbone bus
- FPGA
- PCIe bridge
- ADC
- Analogue front-end
- Clock
- Thermo + ID
- EEPROM
- ADC
- Analogue front-end
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Gateware design tools

**hdlmake: Automating HDL design flow**
- Generates Makefiles for synthesis and simulation.
- Project structure described in Manifest files.
- Solves dependencies (fetches remote ones).

**wbgen2: Wishbone slave generator**
- Describes structure in a single text file.
- Automatically generates HDL source, C header and documentation.
- Generates registers, RAM, FIFO, interrupt controller.

Both FOSS tools available on ohwr.org
Why a new kit

Introduction to OH

OH products

Gateware architecture

New tools

Future work & conclusions

wbgen2: HTML documentation example

---

```
HW prefix: example_csr
HW address: 0x0
C prefix: CSR
C offset: 0x0

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<th>LED_GREEN</th>
<th>SYS_PLL_LCK</th>
<th>FMC_PRES</th>
<th>PCB_REV[3:0]</th>
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</table>

- **PCB_REV** [read-only]: PCB revision
  - Binary coded PCB layout revision.
- **FMC_PRES** [read-only]: FMC presence
  - 0: FMC slot is populated
  - 1: FMC slot is not populated.
- **SYS_PLL_LCK** [read-only]: System clock PLL status
  - 0: not locked
  - 1: locked.
- **LED_GREEN** [read/write]: Green LED
  - Manual control of the front panel green LED (unused in the fmc-adc application)
- **LED_RED** [read/write]: Red LED
  - Manual control of the front panel red LED (unused in the fmc-adc application)
- **RESERVED** [read-only]: Reserved register
  - Ignore on read, write with 0's.
- **TYPE** [read-only]: Carrier type
  - Carrier type identifier
    - 1 = SPEC
    - 2 = SVEC
    - 3 = VFC
    - 4 = SPEXI
```
Testing environment

Production test systems

- Performs automated production tests.
- Includes a software framework to run the tests (Python).
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Future work

Consolidate our designs
- Consolidate documentation (starter guides, ...).
- Continue to transfer knowledge to companies.

Facilitate sharing with FOSS EDA tools
- Tools are expensive and do not interoperate.
- Existing FOSS tools not usable for complex designs.
- We contribute to the development of FOSS tools:
  - Extension of **Icarus** Verilog simulator with VHDL and SystemVerilog support.
  - Enhancement of **KiCAD** (schematics & PCB editor).
Conclusions

- CERN’s FMC kit is not only a set of hardware modules.
  - HDL cores, drivers, test systems, tools
- Eight CERN designs are already commercialized.
- Open Hardware has many advantages.
  - Make better designs: peer review, user feedback
  - More collaborations inside and outside CERN
- OHR site is practical for engineers and is stimulating.
- New users and collaborations are welcome.
- Four years of experience show it works!
Open products are real products™

Want to know more? Take a tour on ohwr.org

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