The White Rabbit Project

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Hardware and Timing section

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1 Introduction

2 Technology
   - Precision Time Protocol (IEEE 1588)
   - Layer 1 syntonization
   - Phase tracking

3 Hardware and applications

4 Conclusions
Outline

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   - Precision Time Protocol (IEEE 1588)
   - Layer 1 syntonization
   - Phase tracking

3. Hardware and applications

4. Conclusions
What is White Rabbit? 1/2

- Ethernet
  - synchronism
  - determinism
What is White Rabbit? 2/2

It is also:

A multi-company, multi-lab collaboration for the development of Open Source SW and HW solutions for controls and DAQ.
Commercial support.
Many users: CERN, GSI, LHAASO, cosmic ray detectors, metrology labs...

The most accurate solution for synchronisation in Ethernet networks.
A candidate to be standardised under IEEE 1588 (PTP).
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Design goals

- Scalability: Up to 2000 nodes.
- Range: 10 km fibre links.
- Accuracy and precision: 1 ns time synchronisation accuracy, 20 ps jitter.
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- DMTD phase tracking.
Network topology

Links are 1Gb/s single fibre (TX and RX use different wavelengths).
Precision Time Protocol (IEEE 1588)

The Precision Time Protocol (PTP) synchronizes local clocks with a master clock by measuring and compensating the delay introduced by the link. This is achieved through frame timestamping, where link delay is measured by exchanging frames with precise hardware transmit/receipt timestamps.
Precision Time Protocol (IEEE 1588)

PTP

Synchronises local clock with the master clock by measuring and compensating the delay introduced by the link.
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Precision Time Protocol (IEEE 1588)

Having values of $t_1 \ldots t_4$, slave can:

- calculate one-way link delay:
  $$\delta_{ms} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$$

- syntonize its clock rate with the master by tracking the value of $t_2 - t_1$

- compute clock offset:
  $$\text{offset} = t_2 - (t_1 + \delta_{ms})$$
Disadvantages of traditional PTP

- All nodes have free-running oscillators.
- Frequency drift has to be continuously compensated, causing lots of network traffic.
- That doesn’t go well with determinism...
Example: Synchronous Ethernet

GPS

System Timing Master

Receiver

Transmitter

Uplink port

Sync-E switch

Receiver

Transmitter

Downlink 1

Transmitter

Downlink 2

Transmitter

Downlink N

Transmitter

Switch fabric

Sync-E node

RX

TX

Other nodes or switches

Reference clock & PPS

Cesium

55

Cs

132.91

Ethernet link

clock loopback
Monitor phase of bounced-back clock continuously.

Phase-locked loop in the slave follows the phase changes measured by the master.
Digital DMTD (Dual Mixer Time Difference)

\[ f_{\text{PLL}} = \frac{n}{n+1} f_{\text{clkA}} \]

\( \text{helper PLL} \)

\( \text{clk}_A \rightarrow \text{clk}_B \)

\( \text{DQ} \)

\( \text{degitcher} \)

\( \text{pulse shaping} \)

\( \text{phase difference averaging} \)

\( \phi \)

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White Rabbit switch v3

Image courtesy of Seven Solutions
Simplified block diagram of WR switch
WR switch FPGA block diagram

- HWIU
- TX TSU
- Pstats
- Endpoint 1..18
- SWCore
- CPU EBI/WB bridge
- RTU
- NIC
- RT subsystem
- VIC
- PWM
- GPIO
- I2C

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Synchronisation performance

Histogram of offsets between master and each slave

- **Master (CH1)**
- **Slave 1 (CH2)**
  - mean: 161.86 ps
  - sdev: 5.45 ps
- **Slave 2 (CH3)**
  - mean: 24.67 ps
  - sdev: 5.30 ps
- **Slave 3 (Ch4)**
  - mean: -135.25 ps
  - sdev: 6.14 ps
PCle FMC carrier
FMC mezzanine: 100 MSPS 14-bit 4-channel ADC
Fine delay generator FMC
Simplified block diagram of a WR node
Inside the FPGA of a WR node

Fiber/Cu → WRPC → FEC → Etherbone

WB core #1 (I/O) → Wishbone interconnect → WB core #3

WB core #2 (CPU+mem) → WB core #3

WB core #4 (host bridge) → WB core #5
Etherbone

Main goals

- Push the customisation layer up by introducing another generic layer on top of WR.
- Very elegant: the whole network is one huge memory map. All messages are reads and writes into some node address space.
- Sits on top of UDP/IP. UDP multi-cast behaves as expected, triggering multiple WB accesses at the same time in many nodes.
Possible applications of White Rabbit

- Large-scale data acquisition systems
- Clock & trigger distribution
- Precise time tagging
- Robust event delivery

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WR in CERN’s BE-CO-HT Hardware Kit

CERN’s BE-CO-HT FMC-based Hardware Kit:

- **FMCs** (FPGA Mezzanine Cards) with ADCs, DACs, TDCs, fine delays, digital I/O.
- Carrier boards in PCI-Express and VME64x formats (a μTCA carrier also exists in the OHR).
- All carriers are equipped with a White Rabbit port.
Distributed Direct Digital Synthesis

- Replaces dozens of cables with a single fibre.
- Works over big distances without degrading signal quality.
- Can provide various clocks (RF of many rings and linacs) with a single, standard link.
Common clock in the entire network: no skew between ADCs.

Ability to sample with different clocks via Distributed DDS.

External triggers can be time tagged with a TDC and used to reconstruct the original time base in the operator’s PC.
The highly deterministic nature of WR networks, coupled with the low latency of the WR switch, make WR an ideal platform for MIMO feedback systems, such as the Fast Orbit Feedback system needed in many synchrotrons.
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Status and outlook

Switches and nodes work and are commercially available. Now working on better diagnostics and remote management for the switch. IEEE 1588 standardisation effort expected to converge in ≈3 years. First operational deployments expected at CERN and elsewhere in 2015.
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A novel networking technology allowing precise synchronisation and deterministic data transfer. A collaborative distributed effort based on open source hardware and software. Everybody is welcome to join! A versatile solution for general control and data acquisition systems. For more information see http://www.ohwr.org/projects/white-rabbit/wiki
A novel networking technology allowing precise synchronisation and deterministic data transfer.
Summary

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- A collaborative distributed effort based on open source hardware and software. Everybody is welcome to join!
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